E E 271 A
Digital Circuits And Systems
Course type: Face-to-Face

Evaluation Delivery: Online
Evaluation Form: A
Responses: 13/19 (68%)

Taught by: Nicole Hamilton, Reza Eghbali, William Lynes
Instructor Evaluated: Nicole Hamilton-Lecturer

Overall Summative Rating represents the combined responses of students to the four global summative items and is presented to provide an overall index of the class's quality:

Combined Median	Adjusted Combined Median
4.6	**4.5**

(0=lowest; 5=highest)

Challenge and Engagement Index (CEI) combines student responses to several *IASystem* items relating to how academically challenging students found the course to be and how engaged they were:

CEI: 5.4

(1=lowest; 7=highest)

SUMMATIVE ITEMS

	N	Excellent (5)	Very Good (4)	Good (3)	Fair (2)	Poor (1)	Very Poor (0)	Median	Adjusted Median
The course as a whole was:	13	46%	46%	8%				4.4	4.3
The course content was:	13	46%	46%	8%				4.4	4.3
The instructor's contribution to the course was:	13	62%	31%	8%				4.7	4.6
The instructor's effectiveness in teaching the subject matter was:	13	62%	23%	15%				4.7	4.6

STUDENT ENGAGEMENT

Relative to other college courses you have taken:	N	Much Higher (7)	(6)	(5)	Average (4)	(3)	(2)	Much Lower (1)	Median
Do you expect your grade in this course to be:	13	23%		46%	23%		8%		4.9
The intellectual challenge presented was:	13	38%	23%	23%	15%				6.0
The amount of effort you put into this course was:	13	38%	31%	15%	8%	8%			6.1
The amount of effort to succeed in this course was:	13	38%	23%	23%	8%	8%			6.0
Your involvement in course (doing assignments, attending classes, etc.) was:	13	38%	46%		15%				6.2

On average, how many hours per week have you spent on this course, including attending classes, doing readings, reviewing notes, writing papers and any other course related work?

Class median: 10.5 Hours per credit: 2.1 (N=13)

Under 2	2-3	4-5	6-7	8-9	10-11	12-13	14-15	16-17	18-19	20-21	22 or more
		8%	15%	23%	8%	15%	8%	15%	8%		

From the total average hours above, how many do you consider were valuable in advancing your education?

Class median: 8.0 Hours per credit: 1.6 (N=13)

Under 2	2-3	4-5	6-7	8-9	10-11	12-13	14-15	16-17	18-19	20-21	22 or more
		8%	38%	15%	8%	8%	15%	8%			

What grade do you expect in this course?

Class median: 3.6 (N=13)

A (3.9-4.0)	A- (3.5-3.8)	B+ (3.2-3.4)	B (2.9-3.1)	B- (2.5-2.8)	C+ (2.2-2.4)	C (1.9-2.1)	C- (1.5-1.8)	D+ (1.2-1.4)	D (0.9-1.1)	D- (0.7-0.8)	E (0.0)	Pass	Credit	No Credit
8%	69%	8%	8%	8%										

In regard to your academic program, is this course best described as:

(N=13)

In your major	A core/distribution requirement	An elective	In your minor	A program requirement	Other
85%		15%			

STANDARD FORMATIVE ITEMS

	N	Excellent (5)	Very Good (4)	Good (3)	Fair (2)	Poor (1)	Very Poor (0)	Median	Relative Rank
Course organization was:	13	54%	31%	15%				4.6	13
Clarity of instructor's voice was:	13	54%	38%	8%				4.6	18
Explanations by instructor were:	13	62%	31%	8%				4.7	14
Instructor's ability to present alternative explanations when needed was:	12	83%	8%	8%				4.9	3
Instructor's use of examples and illustrations was:	13	77%	15%	8%				4.8	5
Quality of questions or problems raised by the instructor was:	13	77%	15%	8%				4.8	1
Student confidence in instructor's knowledge was:	13	92%		8%				5.0	10
Instructor's enthusiasm was:	13	92%		8%				5.0	11
Encouragement given students to express themselves was:	12	75%	17%	8%				4.8	15
Answers to student questions were:	13	69%	8%	23%				4.8	7
Availability of extra help when needed was:	13	69%	15%	8%	8%			4.8	9
Use of class time was:	13	62%	8%	23%	8%			4.7	8
Instructor's interest in whether students learned was:	13	85%	8%	8%				4.9	4
Amount you learned in the course was:	13	54%	38%	8%				4.6	16
Relevance and usefulness of course content were:	13	69%	23%	8%				4.8	6
Evaluative and grading techniques (tests, papers, projects, etc.) were:	12	75%	17%	8%				4.8	2
Reasonableness of assigned work was:	13	62%	31%	8%				4.7	12
Clarity of student responsibilities and requirements was:	12	50%	33%	17%				4.5	17

INSTRUCTOR ADDED ITEMS

	N	Excellent (5)	Very Good (4)	Good (3)	Fair (2)	Poor (1)	Very Poor (0)	Median	
The preparation this course offered for a career in digital design was:	13	46%	54%					4.4	

	N	Strongly Agree (5)	Agree (4)	No Opinion (3)	Disagree (2)	Strongly Disagree (1)	Median	
The overall pace was about right.	13	31%	54%	8%	8%		4.1	
The grading was fair.	13	54%	31%	15%			4.6	
Instructor showed respect for students.	13	85%	15%				4.9	
I would recommend this instructor.	13	62%	31%	8%			4.7	

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STANDARD OPEN-ENDED QUESTIONS

Was this class intellectually stimulating? Did it stretch your thinking? Why or why not?

1. great class. great topic. super powerful and applicable.

2. Yeah.

3. As someone who wants to go into computer science as a major, this class was definitely very stimulating intellectually. I was definitely able to stretch my thinking since I had never done this before.

4. Yes. It introduced me to lots of new things which will be useful to me in the future.

5. Yes, a good introduction to digital circuits and very good presentation of the material. Posing more questions to students would make it even better.

6. It did stretch my thinking in basic FPGA, logics, and FSM. I truly enjoyed learning all these new material.

7. yes

8. I thought this class was an interesting departure from the usual electrical engineering class, we did not deal with voltages, currents, and often did not do any math worse than boolean algebra. it was strange to see logic feedback and how a simple problem in my head such as a counter could quickly turn into 10s of gates in various abstracted blocks

9. Yes, it contains material that is both new and interesting.

What aspects of this class contributed most to your learning?

1. good labs. really did a good job introducing verilog which is complicated and finicky.

2. Examples and her style of going over the style again.

3. I think that the aspects of the class that most contributed to my learning was the instructor's examples and ability to know when students understand the content.

4. Even though I hadn't taken any EE class before, I understood everything thanks to our instructor. She was very friendly and approachable and made the class fun.

5. Example problems, going over some homework problems, extensive lecture slides and lecture notes scanned in which helped me study and review

6. She goes over the same concept multiple times in the beginning of the lecture. That helped me understanding in the fast face lecture.

7. lab

8. i personally liked doing things at the gate level, and always felt good when i understood a block operation like a D flip flop and could start drawing it as a picture box rather than following all the gates the same way every time. i did like hearing about how these gates are built out of transistors and the introduction to computer architecture, even if i got lost in the second one. i did like how the teacher has been in digital design more literally most of its history and knew how it was done on paper back in the 70s as well as other tricks before computers

9. The lab and the lecture

What aspects of this class detracted from your learning?

1. the instructor would take every question and draw it out. with difficult problems that is a very helpful way to show students how to do them. however she took a lot of class time to answer and I think that, often, she would have been better off cutting students off or answering quick questions verbally rather than taking them to the board every time. we could have covered more material if class time was used more efficiently.

2. The classes were long and they were in the evening. I became tired by the end of the class.

3. Nothing except that the chairs in the room were creaky. The instruction did not detract from the learning. However, the chairs should probably be oiled.

4. Nothing

5. 2 and a half hour lecture followed by a long lab makes for an extremely brutal afternoon/night. The labs not having set deadlines wasn't a good idea.

6. fast pace, but as EE major this was expected so I would say it was fair.

7. RAM

8. i realize that verilog is an important piece of this class than cannot be easily done away with and is how most digital design is done now but it was always a difficult part of class. the syntax was not too bad but there is just too much going on to learn well in one class. i personally felt like it was a big departure from logic gates as it slowly became more like a programming language and harder to imagine as gates. i wish we at least went over how to break it back down to the gate level. i am interested in pursuing VLSI and for that will eventually need to go all the way down to the transistor level to "fold" them into a chip. as for the teacher i liked the enthusiasm but i think it showed in a strange way. i could tell she had an idea that got ahead of her words (lots of uuuuuuuu), also people would ask questions and she would try to answer them before the person finished asking and not always answer it the first time. both of these are unflattering things i catch myself doing sometimes and did not like seeing it from somebody else. lastly the 2 hour + lectures really killed me, this is summer quarter so we had to fit a full class into less time which made the pace a bit faster than i would have liked

9. None.

10. Too much emphasis on Verilog, not enough practice with other subject matter from the book.

What suggestions do you have for improving the class?

1. little less time on questions. the stuff from the second half of the class was more interesting. I would have liked more time with those subjects, hard to cover them without the more boring stuff that has to come before tho.

2. I like her teaching style but I guess it would have been more effective if the class was not a summer class because we kinda rushed through at some parts.

3. Not sure if this is a viable suggestion but maybe 3 shorter lectures as opposed to 2 very long lectures since it is hard to pay attention even with a break in between.

4. It is an amazing class already.

5. I'd rather have labs on separate days from the lectures or the lectures broken up into shorter, more frequent chunks. I had to come to school everyday anyway since I was taking a second class as well. Thus, it'd be much easier to digest information and slides would be easier to go through so you don't have to repeat your material that you covered during lecture.

6. maybe some practice exams?? also some more go overs on labs would be great.

7. less content , shorter midterm

8. overall i guess this was a decent beginner level class for digital design and decent for people who just need to take it as an elective

9. None.

10. More strongly correlate hardware implemented with verilog code.

INSTRUCTOR-ADDED OPEN-ENDED QUESTIONS

How did this course affect your thoughts about whether you would like a career in digital design?

1. I never thought about it before, but I am now. Great subject.

3. I don't think that I will have a career in digital design, as I plan to be a CS major, but this class was very enlightening and I'm sure this knowledge will come to use one day.

4. It was exciting to know about all the small elements of a computer, how they work and how people around the world come up with new ideas to increase the efficiency of the circuits. I also want to do something like that in the future.

5. I liked seeing the wide applicability of this course and how relevant it was to everything digital.

7. no

8. i was already considering completing the VLSI concentration as well as sensors and devices to get the deeper semiconductor side of it. overall this has not much changed other than seeing that maybe i do not hate coding as much as i thought i did, just hating java. simply not being scared away from this path yet is probably a good sign

9. I strongly considerate it.

How did the unproctored exams and honor statements affect your experience of the course?

1. Cool. I don't cheat anyway but I like the idea of an honor statement.

2. It was a different experience and it was nice not to have a proctor as I didn't have to be uptight all the time. I was more relaxed.

3. I'm not sure if they affected my experience, but it is a little less distracting to not have someone watch you work at all times, so that was nice.

4. It had no affect on me.

5. Not as much as I thought it would have. It still felt like a testing environment as if the teacher was in the classroom.

6. I want to talk about this. During the exam, some looked under the table for their phones or they went to the bathroom multiple times. I don't think this is fair because they probably searched for answers. You should be in the classroom checking if anyone is cheating.

7. no

8. i honestly cannot say that i have ever had a teacher leave during a test like this. this might become normal later but for these 2 times it felt really strange. i was almost surprised nobody said anything and i did not see any obvious cheating. i almost took my phone out to use as a timer and joked that if we had more time i could have done this evaluation during the test. i did like feeling more trusted. if only they did this in CSE classes then they could take tests on a computer to do a compile check rather than doing it all on paper and making plenty of mistakes.

9. Feel more responsible for my behavior.

10. Unaffected.

What was the most unexpected thing you learned?

1. I guess I wasn't expecting state machines to be so powerful. I really ended up being inspired by the subject.

3. I learned that gates have random delays so some processors for example can roll off the line one day and be better than processors that rolled of the same line the next day.

4. As my first EE class, everything was new and unexpected in some way. System verilog coding was interesting. Also the instructor taught us materials outside the book which was fun and proved to be quite important.

5. Hard to say. I went into this class with absolutely no prior knowledge of gates and flip flops and verilog so I didn't have any expectations going into the course. I guess I could say everything was unexpected, especially with how much the computer world is based off of a 1 or a 0.

9. Fixing code is the most important skill.

10. cisc vs. risc